UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/488,942	01/21/2000	Paul W. Sherer	09764-003531US	5139

7590 04/12/2005

WAGNER MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
DINH, DUNG C	
ART UNIT	**PAPER NUMBER**
2152	

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/488,942	SHERER ET AL.	
	Examiner	Art Unit	
	Dung Dinh	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 6/7/04 have been fully considered but they are not persuasive.

Applicant argued that claim 18 is not obvious over *the publication* because Ethernet and FDDI are not interchangeable. The argument is not persuasive because the Ethernet and FDDI are well known in the art. It is well within the level of an ordinary skill in the art to provide the control circuitry for an Ethernet or FDDI network adapter. The test for obviousness is not whether the features may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). *The publication* teaches to provide buffer threshold interrupt when data in the buffer reaches the threshold. *The publication* discloses that providing programmable threshold allows for early notification yielding absolute minimum frame latencies. (See page 1-2). *The publication* is directed at an FDDI network. However, in view of the teaching as a whole one of ordinary

skill in the art would have been motivated to apply the teaching to an Ethernet controller to achieve the same advantage.

As per claim 22, applicant argued that *the publication* does not teach providing a network driver with early look ahead size. This feature is inherent in a system that make of the AM79C836 chip disclosed in the *publication*. The AM79C836 is a chip for used in a network adapter and provides for early interrupt threshold (i.e. early look ahead size). It is well known in the art that a network driver facilitates communication and data transfer between a computer and a network adapter. A driver is normally designed for a specific hardware so as to isolate the rest of the computer from having to know the specific detail of the hardware. Hence, in a computer system that has a network adapter with the functionality of the AM79C836 chip, it would have been obvious to have the network driver provide means for setting this threshold value in order in order to make use of the early interrupt feature provided by the chip without modification to the rest of the computer system.

The following is a repeat of the prior rejections with added references to support the Examiner assertion that Ethernet control circuitry and Network driver are well known in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 18-21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over AMD's Am79C830 FORMAC Plus as disclosed in "The SUPERNET 2 family for FDDI - 1991/1992 World Network Data Book" (the publication) (Prior art submitted by applicant in parent application file 09/028,088), and further in view of Metcalfe et al. US patent 4,063,220 and Kalwitz US patent 5,696,899.

As per claim 18, the publication discloses a communication adapter with transceiver having transmit buffer, receive buffer, and control circuitry [figure on page 2-4]. The publication discloses readout of a frame while it is being received to reduces delay in waiting for a complete frame [page 2-37, col.1 "Threshold Detection" paragraph]. The publication discloses interrupt circuitry [page 2-36, col.2 "Node Processor (NP) Interface"]. The publication discloses early receive interrupt once a predetermined

number of bytes [threshold] of data packet less than all of said data packet has been received [Apparent from page 2-32 col.1 "INNTERRUPTS. The interrupt signals MINTR1 or MINTR2 ... are asserted when FORMAC Plus status changes", page 2-52 col.2 "The receive frames are loaded into the buffer memory ... for single-frame receive mode ... The RDATA timing depends upon the receive threshold value...", page 2-64 bottom of col.1 "the ST2 register contains status bit that may generate maskable interrupts on the MINTR2 pin", bottom of col.2 "Receive Frame. RSCVRM (bit10) - This bit is set, during single-frame receive-mode operation, to interrupt the NP and indicate that data is present in the buffer memory"].

The publication does not teach Ethernet control circuitry and host adapter interface. The publication teaches the chip for use in an FDDI network. However, specific type of network (Ethernet vs. FDDI) would have been an obvious variation from the teaching of the publication. Ethernet and token ring such as FDDI are notoriously well known in the art at the time of the invention and can often be used together. (See Kalwitz col.11 lines 1-8). Ethernet is a popular protocol for a local area network. The publication discloses that providing programmable threshold allows for early notification yielding absolute minimum frame latencies. (see page 1-2). Hence, it would have been obvious for one of

ordinary skill in the network adapter art to adapt the features of the AM79C830 chip disclosed in the publication to an Ethernet adapter because it would have provided the equivalent improvement to the processing of Ethernet data packets. The Ethernet control circuitry and host interface are well known to one of ordinary skill in the art of network adapter design. (See the Metcalfe's Ethernet patent 4,063,220). Hence, in applying the features of the AM79C830 chip to an Ethernet network adapter, it is expected and is well within the skill of one of ordinary skill in the art to provide the Ethernet control circuitry and host interface.

As per claim 19, The AM79C830 is contained in a single application specific integrated circuit (ASIC). The publication does not specifically teach Ethernet control circuitry. However, it would have obvious for one of ordinary skill in the art to apply the early interrupt to a Ethernet control circuitry because it would have reduces delay in waiting for a complete Ethernet frame thereby provided an improved Ethernet network adapter.

As per claim 20, the publication discloses the threshold is programmable [page 2-97 "Frame Threshold Register - FRMTHR"].

As per claim 21, the publication discloses the circuit is programmable to generating a packet transmit signal when the buffer contains a predetermined number of bytes [page 2-98 col.1 "Transmit Threshold. XTHR"].

As per claims 22, the publication discloses method of transferring a packet of data comprising the steps of:

a) receiving from the communication media and storing in a receive buffer a first threshold number of bytes of the packet [page 2-37, col.1 "Threshold Detection"];

b) thereupon generating a first early interrupt from the adapter to the host computer [apparent from page 2-52 col.2 "The receive frames are loaded into the buffer memory ... for single-frame receive mode ... The RDATA timing depends upon the receive threshold value..."; page 2-64 bottom of col.1 "the ST2 register contains status bit that may generate maskable interrupts on the MINTR2 pin"; bottom of col.2 "Receive Frame. RSCVRM (bit10) - This bit is set, during single-frame receive-mode operation, to interrupt the NP and indicate that data is present in the buffer memory"];

c) thereafter receiving from the communication media and storing in the receive buffer a remainder of the packet [page 2-37, col.1 "Threshold Detection" - "...read out of the frame can then take place at the same time that the frame is being written"].

The publication does not specifically disclose the host employing a driver allowing for early indication. It is well

known in the art to employ network driver to facilitate communication to a network adapter. (See Kalwitz figs 6 and 7, col.27 lines 8-12). The function of a driver is to provide software interface to the hardware so that changes to hardware only need changes to the driver; not to the rest of the computer system. Hence, it would have been obvious that a system having a network adapter using the AM79C830 chip would have had a driver for interfacing this network adapter to the host computer. Since one of the advantages of the AM79C830 chip the programmable early notification (see publication page 1-2), it would have been obvious for one of ordinary skill in the art to provide a look ahead size (e.g. a threshold value) with the driver because it would have enabled the driver to set and control the early notification so as to make full use of the AM79C830 capabilities.

Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over the Am79C830 publication, Kalwitz, and further in view of Firoozman US patent 5,210,749.

As per claim 23, the publication does not disclose determining the threshold value based on the latency of the host computer and the network. In similar field of invention, Firoozman teaches determining the threshold value based on the latency of the host computer and the network (col.14 lines 55-64).

It would have been obvious for one of ordinary skill in the art to use Firoozman teaching with the Am79C830 publication because Firoozman teaches an improvement on the application of the Am79C830 chip (see col.1 lines 29-37).

Claim 24 and 25 are rejected under 35 U.S.C. § 103 as being unpatentable over the Am79C830 publication, Kalwitz, and Firoozman and further in view of Bentley et al. patent 4,860,193.

As per claims 24 and 25, the publication and Firoozman do not specifically teach adjusting the threshold. However, the publication discloses the threshold is programmable (see page 1-2). Furthermore, in similar field of invention, Bentley teaches adjusting the buffer threshold according to previous data block length to better adapt the buffer to the data length so as to reduce latency. Therefore, it would have been obvious for one of ordinary skill in the art to adjust the threshold value so as to maximize throughput and reduce latency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung Dinh whose telephone number is (571) 272-3943. The examiner can normally be reached on Monday-Friday from 7:00 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached at (571) 272-3949.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dung Dinh
Primary Examiner
April 5, 2005